AMENDMENTS

Amendments to the Specification:

Please replace paragraph [0027] with the following amended paragraph:

In one exemplary embodiment, packet processing system 200 may be a line card in a WAN connecting a data stream from Ethernet to SONET. In this embodiment, the line card is coupled to an optic network medium (network medium 270) and a copper medium (medium 280) by lines 215 and 211, respectively. The copper medium may include multiple serial ports. The copper medium is coupled to an Ethernet device (physical interface device 290) of the line card by line 211. The Ethernet device acts as a serializer/deserializer (SERDES) and may be a backbone link between multiple line cards. The Ethernet device is coupled to the link layer device 250 by line 212. In such an exemplary embodiment, the link layer device 250 may utilize a FPGA device as processing device 251. In this exemplary embodiment, packet processing functions, such as encapsulating the data into a communication protocol, such as ATM, GFP, and HDLC, that may be performed in processing device 251, are performed by the framer 240. The framer 240, acting as master device, receives isolated input data packets and frames the data to be output as back-to-back framed data to the SONET device (physical interface device [[260_1]] 260) on line 214 (described in detail below). The SONET device transmits the framed data over the optic medium (network medium 270) on line 215. In another embodiment, multiple packet processing systems may be implemented in multiple line cards, each line card including a framer and a SONET device coupled to a network medium, and the line cards may be coupled to each other through a backbone physical interface. In an alternative embodiment, the operations discussed below in the context of framer 240 may be performed in other devices, such as, for example, a network processor, co-processor, encapsulator, or switch.

Please replace paragraph [0033] with the following amended paragraph:

Figure 4 illustrates one embodiment of CRC computation circuitry having CRC calculators and nullifiers. In this embodiment, CRC computation circuitry 360 includes a single CRC calculator 410, a plurality of CRC nullifiers 420_1 to 420_{N-1} and multiplexers (MUX) 430, 440 and 450. The inputs to the multiplexer 430 include a data byte (DataByte_N) input signal 401 and a feed zero input signal 402. The output of multiplexer 430 is controlled by a byte enable (ByteEn_N) signal 407. The inputs to the multiplexer ~~403~~ 440 include a default value input signal 403, and a CRC input signal 408 that is coupled to receive the output of the CRC calculator 410. The output of the multiplexer 440 is controlled by the CRC reset or start of packet signal 405. The outputs of multiplexers 430 and 440 are coupled to the CRC calculator 410. In one embodiment, the output of the CRC calculator 410 is coupled to the output multiplexer 450 and to the CRC nullifiers 420_1 to 420_{N-1}, where N is the width of the input data bus 490, in bytes. The outputs of the CRC nullifiers are coupled to output multiplexer 450. The output multiplexer 450 is controlled by a byte enable signal 406. The output from multiplexer 450 is the final CRC out value. The operation of the CRC computation circuitry 360 is discussed below in relation to Figure 7. Multiplexers, CRC calculators and nullifiers are known in the art[[;]]. ~~according~~ Accordingly, a more detailed description is not provided.